REMARKS

Claims 1-13 are pending. By this Amendment, the specification and claims 1 and 12 are amended. Reconsideration based on the above amendments and following remarks is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten paragraph (37 C.F.R. §1.121(b)(1)(iii)) and claim (37 C.F.R. §1.121(c)(1)(ii)).

Applicant gratefully acknowledges that the Office Action indicates that claim 7 is allowed.

I. THE SPECIFICATION SATISFIES ALL FORMAL REQUIREMENTS

Although not objected to by the Examiner, the specification is amended to correct informalities. No new matter has been added.

II. THE CLAIMS DEFINE ALLOWABLE SUBJECT MATTER

The Office Action rejects claims 1-2 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,767,827 to Kobayashi et al. (hereinafter "Kobayashi") in view of U.S. Patent No. 6,124,912 to Moore (hereinafter "Moore") and U.S. Patent No. 5,805,252 to Shimada et al. (hereinafter "Shimada"); claims 3 and 8-9 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,510,918 to Matsunaga et al. (hereinafter "Matsunaga") in view of Moore; claim 4 under 35 U.S.C. §103(a) as unpatentable over Kobayashi in view of Matsunaga; claims 5-6 under 35 U.S.C. §103(a) as unpatentable over Kobayashi in view of Matsunaga, and further in view of Moore; and claims 10 and 12 under 35 U.S.C. §103(a) as unpatentable over Matsunaga. The rejections are respectfully traversed.

Regarding Moore, Applicant respectfully submits that Moore was wrongly applied as "prior art" in rejecting claims 1-3, 5, 6, 8, 9, 11 and 13. This application claims priority from Japanese Application JP A 8-279388, which priority date of October 22, 1996 and

which predates Moore's effective prior art date. A certified English-translation copy of JP A 8-279388, which fully supports all features of claims 1 and 3, is attached herein for examination.

Regarding claim 1, as discussed above, all features of this claim are supported in JP 388, and thus Moore does not constitute "prior art". Also, Kobayashi does not teach, disclose or suggest a silicon nitride film formed as an insulating interlayer between said reflecting electrodes and a metal layer, as recited in claim 1. Instead, Kobayashi shows an insulating film 7a and 7b in Fig. 1, which is a silicon oxide film. Further, Shimada does not make up for these deficiencies. Instead, Shimada discloses a gate insulating film 5 which is different from the silicon nitride film above the switching element, as recited in claim 1.

Regarding claim 3, as discussed above, all features of this claims are supported in JP 388, and thus Moore does not constitute "prior art". Thus, Moore is not a valid reference with regard to claim 3. Also, regarding claim 3, Matsunaga does not teach, disclose or suggest a passivation film having a laminate structure comprising a silicon oxide film and a silicon nitride film on said silicon oxide film, the passivation film being formed at edge sections of the metal layer and the insulating interlayer, as recited in claim 3. Instead, Matsunaga discloses that a passivation film PSV1 (one of silicon oxide and silicon nitride) is formed in series manner on matrix portion AR and peripheral region.

Regarding claim 4, Kobayashi does not teach, disclose or suggest a first passivation film comprising a silicon oxide film formed on said reflecting electrodes in said pixel region; and a second passivation film comprising a silicon nitride film formed on said periphery region, as recited in claim 4. Instead, Kobayashi discloses that a passivation film (oxide film) 11 is formed on display pixel area 17 and on the single-drive scanning circuit 18, as shown in Figs. 7 and 8.

Matsunaga does not make up for these deficiencies. Instead, Matsunaga discloses that a passivation film PSV1 (one of silicon oxide and silicon nitride) is formed in series manner on matrix portion AR and peripheral region.

Regarding claim 4, a pixel region has a first passivation film comprising a silicon oxide so that changes in reflectance of the reflection electrode are reduced, and a peripheral region has a second passivation film comprising a silicon nitride for improving moisture resistance. Kobayashi and Matsunaga, individually or in combination, do not render obvious the combination of a silicon oxide film on the reflecting electrode and silicon nitride film on the peripheral region, as recited in claim 4.

Regarding claim 10, Matsunaga does not teach, disclose or suggest a passivation film formed by a silicon nitride film having moisture resistance and formed on a scribed region of said semiconductor substrate, as recited in claim 10. Instead, Matsunaga teaches a substrate which is not a semiconductor, but a glass. Furthermore, Matsunaga discloses a passivation film PSV1, which passivation film PSV1 is not formed on a scribed region of the substrate, as recited in claim 10. Rather, Matsunaga's passivation film PSV1 terminates before the scribed region of the substrate.

Likewise, regarding claim 12, Matsunaga does not teach, disclose or suggest the passivation film extending on a scribed region of the first substrate, as recited in claim 12. Instead, Matsunaga's passivation film PSV1 terminates before the scribed region of the substrate. Accordingly, the passivation film PSV1 of Matsunaga is not formed on the subscribed region of the substrate.

For at least the reasons, it is respectfully submitted that claims 1, 3, 4, 10 and 12 are distinguishable over the applied art. Claims 2, 8-9, 5-6, 11 and 13, which depend from claims 1, 3, 7, 10 and 12, respectively, are likewise distinguishable over the applied art for at least the reasons discussed, as well as for the additional features they recite. Withdrawal of the rejections under 35 U.S.C. §103(a) is respectfully requested.

III. CONCLUSION

For at least the reasons discussed above, it is respectfully submitted that this application is in condition for allowance.

Should the Examiner believe that anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Registration No. 27,075

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JAO:RJK/sld

Attachments:
Appendix
Petition for Extension of Time
Certified English Translation of JPA 8-279388

Date: August 19, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Specification:

Page 8, line 29 - page 9, line 5:

On the substrate surface in the other opening formed in the field oxide film 3, a P-type doping region 8 is formed. On the surface of the P-type doping region 8, an electrode 9a composed of polysilicon or metal silicide is formed through an insulating film 9b formed by thermal oxidation. A capacitor for holding a voltage applied to the pixel is formed between the electrode 9a and the P-type doping region 8 through the insulating film ~~9~~ 9b. The electrode 9a and the polysilicon or metal silicide layer as the gate electrode 4a of the MOSFET can be formed by the same process, and the insulating film 9b under the electrode 9a and the insulating film as the gate insulating film 4b can be formed by the same process.

Page 11, line 35 - page 12, line 11:

In this embodiment, a third insulating layer 13 is formed on the light shielding layer 12, and a rectangular pixel electrode 14 as a reflective electrode almost corresponding to one pixel is formed on the third insulating layer 13 as shown in Figure 3. A contact hole 16 is provided inside the opening 12a in the light shielding film 12 so as to pierce the third insulating interlayer 13 and the second insulating interlayer 11, and the contact hole 16 is filled with a pillar connecting plug 15 composed of a high melting point metal, such as tungsten, which electrically connects the auxiliary bonding wire 10 and the pixel electrode 14. A passivation film 17 is formed on the entire pixel electrode 14.

Page 30, line 10 - page 31, line 2:

Figure 17 is a cross-sectional view of a configuration of a pixel in a reflective liquid crystal panel substrate. Figure 17 is a cross-sectional view along line I-I in the planar layout in Figure 3, as in Figure 1. In this embodiment, a TFT is used as a transistor for switching pixels. In Figure 17, the sections having the same identification numbers as Figures 1 and 2

represent the layers and the semiconductor regions having the same functions as in those drawings. Identification number 1 represents a quartz or non-alkaline glass substrate, single-crystal, polycrystalline or amorphous silicon film, regions 5a, 5b, 5c and 8 are formed on the insulating substrate, and insulating films 4b and 9b having a double layer structure composed of a silicon oxide film formed by thermal oxidation and a silicon nitride film formed thereon by a CVD process are formed on the silicon film. An N-type impurity is doped in the regions 5a, 5b and 8 of the silicon film before the formation of the upper silicon nitride film among the insulating film 4b to form a source region 5a and a drain region 5b of the TFT and an electrode region 8 of the holding capacitor. A wiring layer composed of polysilicon or a metal silicide is formed as a gate electrode 4a of the TFT and the other electrode 9a of the holding capacitor is formed on the insulating film 4b. As described above, the TFT comprising the gate electrode 4a, the gate insulating film 4b, the channel 5c, the source 5a and the drain 5b and the holding capacitor comprising the electrodes 8 and 9a and the insulating film 9b are formed.

IN THE CLAIMS:

The following are marked-up versions of the amended claims:

1. (Amended) A liquid crystal panel substrate, comprising:

reflecting electrodes formed on a substrate;

a switching element formed corresponding to each of the reflecting electrodes;

a passivation film formed on said reflecting electrodes comprising a silicon oxide film; and

a silicon nitride film formed as an insulating interlayer between said reflecting electrodes and a metal layer above the switching element thereunder having moisture resistance.

12. (Amended) A liquid crystal panel, comprising:

_____a first substrate;~~,~~

_____a second substrate opposed to the first substrate;~~,~~

_____a liquid crystal therebetween, and

_____a seal material sealing the first substrate and the second substrate;~~, the liquid crystal panel further comprising:~~

a pixel region having reflecting electrodes formed on said first substrate; and

a passivation film comprising a silicon nitride film formed in a region arranged with said seal material on said first substrate, the seal material being formed on the silicon nitride, and the passivation film extending on a scribed region of the first substrate.